R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR AMENDMENT TO THE SPECIFICATION

Support for the amendment to the specification can be found in the drawings as originally filed, for example, in FIGS. 2-3 and in the specification as originally filed, for example, on page 6, lines 1-9, on page 8, lines 3-16 and on page 9, lines 4-6 and lines 17-19. Specifically, the specification states:

> **Pinout may refer to a layout of the signals for a device** (e.g., a list of physical pins of a device package and functions assigned to those pins). For example, **a pinout may be a list of pins and pin functions** for quad flat pack (QFP) (e.g., pin1 = ground, pin2 = signal A, etc.) and **for a ball grid array** (BGA) (e.g., A1=Ground, A2 = signal A, etc.) Pinlist may refer to a list of signals for a device to be assigned to physical pins to become the functions of the pins (e.g., the ground, signal A, etc.). **For simplicity a BGA ball may also be referred to as a pin** (page 6, lines 1-9 of the specification as originally filed, emphasis added).

The specification further states:

> While in the state 58, the process 50 may mark pins associated with each member after the pinout is completed. **The process 50 may generate a pinout specific to a particular device member by marking (or customizing) the superset grid for each member using information generated at the state 54** (e.g., information regarding which pin is applicable to which device). For example, a single A may be applicable to both members MEMBERA and MEMBERB, while C may be applicable to member MEMBERA. Pins not applicable to a particular

> member device may be marked "no-connect" for the device. Users may then optionally ignore the no-connect pins if using one specific member of the family. Therefore, the process 50 may provide a footprint that may be common to all members in the family and a superset pinout that accommodates the needs of all members (page 8, lines 3-16 of the specification as originally filed, emphasis added).

and

> Referring to FIG. 2, **a block diagram of system (or circuit) 100 is shown** illustrating an implementation of the process 50 (or 50'). **The circuit 100 may be a BGA layout.**
>
> ***
>
> Referring to FIG. 3, **a circuit 100' is shown** illustrating an implementation of the process 50 (or 50'). **The circuit 100' may be a BGA layout**. (page 9, lines 4-19 of the specification as originally filed, emphasis added).

A person of ordinary skill in the relevant art, reading the specification as originally filed, would recognize FIGS. 2 and 3 as illustrating superset grids. As such no new matter has been added.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, in FIGS. 1a-3 and in the specification as originally filed, for example, on page 5, line 10 through page 9, line 16, and on page 10, line 7 through page 12, line 4. As such no new matter has been added.

OBJECTIONS TO THE SPECIFICATION

The objection to the title is respectfully traversed and should be withdrawn. The current title "METHOD AND/OR ARCHITECTURE FOR GENERATING SUPERSET PINOUT FOR DEVICES WITH COMBINED PROGRAMMABLE LOGIC AND HIGH-SPEED SERIAL CHANNELS" is believed to be compliant with MPEP §606. Specifically, the present title contains fewer than 500 characters, is believed to be technically correct and is descriptive. In particular, claim 1 recites "A method for generating a superset pinout for a family of devices" and claim 4 which depends directly from claim 1 recites "said family of devices comprises devices with combined programmable logic and high-speed channels." Therefore, the title clearly is directed to the subject matter presently claimed. Since the title appears to reflect the claimed invention, the title appears to be both technically accurate and descriptive as required by MPEP §606. As such, the objection to the title does not appear to be proper and should be withdrawn. However, if the Examiner chooses to maintain the objection to the title, Applicant's representative respectfully requests that the Examiner suggest a title that would be acceptable.

The objection to the specification as not making the meaning and relevance of the term "superset grid" apparent has been obviated by appropriate amendment and should be withdrawn. Specifically, the specification has been amended to indicate that the grids of FIGS 2 and 3 illustrate superset grids as presently claimed.

The objection to the specification as not disclosing the meaning and relevance of the phrase "increased bandwidth channels" as recited in claim 18 is respectfully traversed. Specifically, claim 18 does not recite the phrase "increased bandwidth channels." However, if the objection was meant to refer to claim 17, a person of ordinary skill in the relevant are would recognize the specification as disclosing the meaning and relevance "increased bandwidth channels." In particular, the specification as originally filed recites, *inter alia*, that:

> The process 50 (or 50') may generate a superset pinout for a family of programmable serial interface (PSI) devices. The process 50 (or 50') may allow for different gate densities and different numbers and functions of transceiver channels to be accommodated by a superset pinout. **The process 50 (or 50') may provide a user with a PSI device design migration path to** higher CPLD gate densities and **more SERDES transceiver bandwidth** within a common footprint. The process 50 (or 50') may eliminate footprint changes when users replace a device with another having a different programmable logic gate density while in the same family, since a common footprint exists for the two members. **The process 50 may eliminate footprint changes when users replace a device with another having a different number of high-speed serial channels while in the same family, since a common footprint exists for the two members** (page 11, lines 3-15 of the specification as originally filed, emphasis added).

Therefore, since a person of ordinary skill in the relevant are would recognize the specification as disclosing the meaning and relevance of the phrase "increased bandwidth channels," the objection does not appear to be proper and should be withdrawn.

CLAIM OBJECTIONS

The objections to claims 1, 2, 9, 10, 13, 15-19 and 20 are, in part, obviated by appropriate amendment and, in part, respectfully traversed. As such, the objections should be withdrawn.

Specifically, the objections with respect to claims 2, 9, 10, and 13 have been obviated by appropriate amendment and should be withdrawn.

The objection to claims 1, 19 and 20 with respect to the clarity of "marking each pin" is respectfully traversed and should be withdrawn. Specifically, the specification as originally filed recites:

> While in the state 58, the process 50 may mark pins associated with each member after the pinout is completed. The process 50 may generate a pinout specific to a particular device member by marking (or customizing) the superset grid for each member using information generated at the state 54 (e.g., information regarding which pin is applicable to which device). For example, a single A may be applicable to both members MEMBERA and MEMBERB, while C may be applicable to member MEMBERA. Pins not applicable to a particular member device may be marked "no-connect" for the device. Users may then optionally ignore the no-connect pins if using one specific member of the family. Therefore, the process 50 may provide a footprint that may be common to all members in the family and a superset pinout that accommodates the needs of all members (page 8, line 3 through page 9, line 3 of the specification as originally filed).

A person of ordinary skill in the relevant art, reading the claims in light of the specification, would be able to reasonably ascertain how and with what each pin may be marked based on the

specification as originally filed. As such, the objection does not appear to be proper and should be withdrawn.

The objection to claim 20 with respect to the claims structure (see page 3, lines 3-7 of the Office Action) has been obviated by appropriate amendment and should be withdrawn.

The objection to claims 15-18 under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112, FIRST PARAGRAPH

The rejection of claims 19 and 20 under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112, SECOND PARAGRAPH

The rejection of claim 10 under 35 U.S.C. §112, second paragraph, as being indefinite has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1, 9, 10, 15 and 20 under 35 U.S.C. §103(a) as being unpatentable over Malhotra et al. (U.S.

Patent No. 6,320,410; hereinafter Malhotra) is respectfully traversed and should be withdrawn.

In contrast to Malhotra, the present invention provides a method for generating a superset pinout for a family of devices, comprising the steps of: (A) defining a pinlist for each device within said family of devices, wherein said family of devices comprises devices having either (i) different numbers of high-speed transceiver channels, (ii) different functions of high-speed transceiver channels or (iii) different numbers and functions of high-speed transceiver channels; (B) generating a superset listing of pins from said pinlist for each device within said family of devices; (C) creating said superset pinout for said family of devices from said superset listing of pins to eliminate potential footprint variations within said family of devices; and (D) marking each pin of said superset pinout associated with each member of said family of devices. Claims 19 and 20 recite similar limitations. The Office Action fails to meet the Office's burden to factually establish that Malhotra teaches or suggests each and every element of the presently claimed invention (MPEP §2142). As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Specifically, the Office Action states "Malhotra does not explicitly disclose the creation of a superset pin listing or a superset pinout. Nor does Malhotra explicitly disclose the marking of pins." Therefore, The Office Action admits that Malhotra does not explicitly teach or suggest each and every element of the

presently claimed invention. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, the Office Action fails to present evidence or a convincing line of reasoning why a person of ordinary skill in the relevant art would view Malhotra as implicitly teaching or suggesting each and every element of the presently claimed invention. In particular, assuming, *arguendo*, the TABLE 1 of Malhotra could be compared to the presently claimed pinlist for each device within the family of devices (as suggested on page 5, section 13 of the Office Action and for which Applicant's representative does not necessarily agree), the Office Action presents no evidence or convincing line of reasoning that one of ordinary skill in the art would consider a listing of some density and package combinations offered within a particular family as shown in TABLE 1 of Malhotra (see column 1, lines 19-21 of Malhotra) as being the same as the presently claimed pinlist for each device with in the family of devices.

Specifically, the specification (see page 6, lines 6-8) states that "Pinlist may refer to a list of signals for a device to be assigned to physical pins to become the functions of the pins (e.g., the ground, signal A, etc.)." Since the TABLE 1 of Malhotra does not appear to list signals for the different parts, it follows that one of ordinary skill in the art would not consider TABLE 1 of Malhotra as being the same as the presently claimed pinlist for each device with in the family of devices. Therefore, the Office

Action fails to meet the Office's burden to factually establish a *prima facie* case of obviousness by present prior art references that teach or suggest **each and every element** of the presently claimed invention (MPEP §2142). As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Furthermore, the Office Action fails to present evidence or a convincing line of reasoning why a person of ordinary skill in the relevant art would view Malhotra as implicitly teaching or suggesting creating a superset pinout as presently claimed. In particular, assuming, *arguendo*, the TABLE 2 of Malhotra could be compared to the presently claimed superset pinout for the family of devices (as suggested on page 5, section 13 of the Office Action and for which Applicant's representative does not necessarily agree), the Office Action presents no evidence or convincing line of reasoning that one of ordinary skill in the art would consider a listing of 16 logic blocks of a particular design, with the number of I/O macrocells that are contained within each logic block as shown in TABLE 2 of Malhotra (see column 2, lines 23-30 of Malhotra) as being the same as the presently claimed superset pinout for the family of devices.

Specifically, the specification (on page 6, lines 1-6) states:

> Pinout may refer to a layout of the signals for a device (e.g., a list of physical pins of a device package and functions assigned to those pins). For example, a pinout may be a list of pins and pin functions for quad flat

> pack (QFP) (e.g., pin1 = ground, pin2 = signal A, etc.) and for a ball grid array (BGA) (e.g., A1=Ground, A2 = signal A, etc.).

Since the TABLE 2 of Malhotra does not appear to list either signals or physical pins of a device package and functions assigned to those pins for the different parts, it follows that one of ordinary skill in the art would not consider TABLE 2 of Malhotra as being the same as the presently claimed superset pinout for the family of devices. Therefore, the Office Action fails to meet the Office's burden to factually establish a *prima facie* case of obviousness by present prior art references that teach or suggest **each and every element** of the presently claimed invention (MPEP §2142). As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

The Office Action similarly fails to present any evidence or convincing line of reasoning that one of ordinary skill in the art would not consider TABLE 2 of Malhotra as teaching or suggesting marking each pin of the superset pinout, as presently claimed (see page 5, section 13 of the Office Action). Therefore, the Office Action fails to meet the Office's burden to factually establish a *prima facie* case of obviousness by present prior art references that teach or suggest **each and every element** of the presently claimed invention (MPEP §2142). As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2-4, 6-11, 13-18 depend, directly or indirectly, from claim 1 which is believed to be allowable. As such, the presently claimed invention is fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative, Robert Miller, should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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